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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/752,386	HORAK ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *13-17* is/are withdrawn from consideration.

5)☒ Claim(s) *8 and 10-12* is/are allowed.

6)☒ Claim(s) *1-7,9 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-4, 6, 7, 9 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 12-13, the phrase "using said spacer, during the implanting step, to mark said substrate from the ions used in said implanting step" is vague and indefinite. Fig. 3 shows the spacer [26] is used as a mask to implant ions into the substrate [10]. It is believed that the phrase should rewrite as "using said spacer, during the implanting step, to mask said substrate from the ions used in said implanting step".

Claim 9, line 2, the phrase "source and drain regions extensions" is unclear whether it is being referred to the source and drain extension regions of claim 8.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 4 and 18 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Yeap et al.

In regards to claim 1, Yeap et al. show all the elements of the claimed invention in figs. 10-18. It discloses a method of forming a doped gate structure on a semiconductor device [60], comprising the steps: providing a semiconductor device [60] including a substrate [62] and a gate dielectric layer [66] on said substrate; forming a gate stack

[64, 68] on said dielectric layer [66], including the steps of forming a first gate layer [64] on the dielectric layer, and forming a second gate layer [68] on top of the first gate layer; forming a spacer (a lower portion of layer [84] ([88] in fig. 15)) around the first and second layers [64, 68]; and removing the second layer [68]; using said spacer (a lower portion of layer [84] ([88] in fig. 15)), during an implanting step, to mask said substrate [62] from ions used in said implanting step.

Since Yeap et al. never disclose any mask layer formed above the gate electrode [64] in figs. 15 and 16, the entire device is being exposed to the ions during the ion implantation process. Therefore, the first gate layer [64] is also implanted with ions by directing said ions directly into the first gate layer [64] during the source/drain regions [90, 92] implantation step. Therefore, a doped gate layer [64] formed above the gate dielectric layer [66].

In regards to claim 2, Yeap et al. further disclose the spacer is a first spacer, and further comprising the steps of: removing a portion of the first spacer (from [84] to [88], figs. 14 and 15); forming a second spacer [70], thinner than the first spacer, around the first gate layer [64]; and implanting further ions (the ions in regions [72, 74]) in the semiconductor device, around a portion of the second spacer [70], to form source and drain extension regions [100, 102] in the semiconductor device, around the second spacer [70].

In regards to claim 4, Yeap et al. further disclose the step of: forming a third spacer [82] around a portion of the first gate layer [64] and above the source and drain extension regions [100, 102].

In regards to claim 18; Yeap et al. further disclose the implanting step includes the step of implanting said ions in the first gate layer [64] while keeping the spacer around the first gate layer [64].

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeap et al.

In regards to claim 6, Yeap et al. differ from the claimed invention by not showing the spacer is comprised of silicon oxide.

It would have been obvious for the spacer is silicon oxide because it is a conventional sidewall spacer material. It also would have been obvious for the spacer comprised of silicon oxide, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

In regards to claim 7, Yeap et al. differ from the claimed invention by not showing the first gate layer has a height of about 150 nm and the second layer has a height of about 150 nm.

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first gate layer has a height of about 150 nm and the second layer has a height of about 150 nm, since it has been held that discovering an optimum

value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d272, 205 USPQ 215 (CCPA 1980). In addition, it also depends on the desired size of the device.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 5, 6 and 18 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Moslehi.

In regards to claim 1, Moslehi shows all the elements of the claimed invention in figs. 2-9. It discloses a method of forming a doped gate structure on a semiconductor device [36], comprising the steps: providing a semiconductor device [36] including a substrate [38] and a gate dielectric layer [48] on said substrate; forming a gate stack [50, 52, 54] on said dielectric layer [48], including the steps of forming a first gate layer [50] on the dielectric layer, and forming a second gate layer [54] on top of the first gate layer; forming a spacer [56] around the first and second layers [50, 54]; and removing the second layer [54] (fig. 6); and implanting ions in the first gate layer [50] by directing said ions directly into the first gate layer [50] (col. 13, lines 24-36) to form a doped gate [50] above the gate dielectric layer [48]; and using said spacer [56], during the implanting step, to mask said substrate from the ions used in said implanting step (fig. 4).

In regards to claim 6, Moslehi further discloses the spacer [56] is comprised of silicon oxide (col. 12, lines 23-24).

In regards to claim 18, Moslehi further discloses the implanting step includes the step of implanting said ions in the first gate layer [50] while keeping the spacer [56] around the first gate layer [50].

In regards to claim 5, Moslehi shows all the elements of the claimed invention in figs. 2-9. It discloses a method of forming a doped gate structure on a semiconductor device [36], comprising the steps: providing a semiconductor device [36] including a substrate [38] and a gate dielectric layer [48] on said substrate; forming a gate stack [50, 52, 54] on said dielectric layer [48], including the steps of forming a first gate layer [50] on the dielectric layer, and forming a second gate layer [54] on top of the first gate layer; forming a spacer [56] around the first and second layers [50, 54]; and removing the second layer [54] (fig. 6); and implanting ions in the first gate layer [50] by directing said ions directly into the first gate layer [50] (col. 13, lines 24-36) to form a doped gate [50] above the gate dielectric layer [48]; and using said spacer [56], during the implanting step, to mask said substrate from the ions used in said implanting step (fig. 4) wherein: the first gate layer [50] is comprised of polysilicon (col. 11, lines 32-33); and the second layer [54] is comprised of polygermanium (polycrystalline germanium) (col. 11, lines 28-45, col. 12, lines 1-6).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moslehi.

In regards to claim 7, Moslehi differs from the claimed invention by not showing the first gate layer has a height of about 150 nm and the second layer has a height of about 150 nm.

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first gate layer has a height of about 150 nm and the second layer has a height of about 150 nm, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d272, 205 USPQ 215 (CCPA 1980). In addition, it also depends on the desired size of the device.

9. Claims 8 and 10-12 are allowed.

10. Applicant's arguments filed 11/22/05 have been fully considered but they are not persuasive.

It is urged, in page 11 of the remarks, that in Yeap, the spacer around the gate stack is used to protect that gate stack when the substrate is doped, while with the instant invention, the spacer around the gate stack is used to mask the semiconductor substrate when the gate stack is doped. However, Yeap also shows the spacer (a lower portion of [84] ([88] in fig. 15)) around the gate stack [64, 68] is used to mask the semiconductor substrate when the gate stack is doped in figs. 14-16.

It is urged, in page 12 of the remarks, that Moslehi never discloses the spacer is used to mask the semiconductor substrate while the gate stack is doped. However, Moslehi also shows the spacer [56] is used to mask the semiconductor substrate [38] while the gate stack [50, 52, 54] is doped.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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February 1, 2006

Steven Loke
Primary Examiner
Steven Loke